

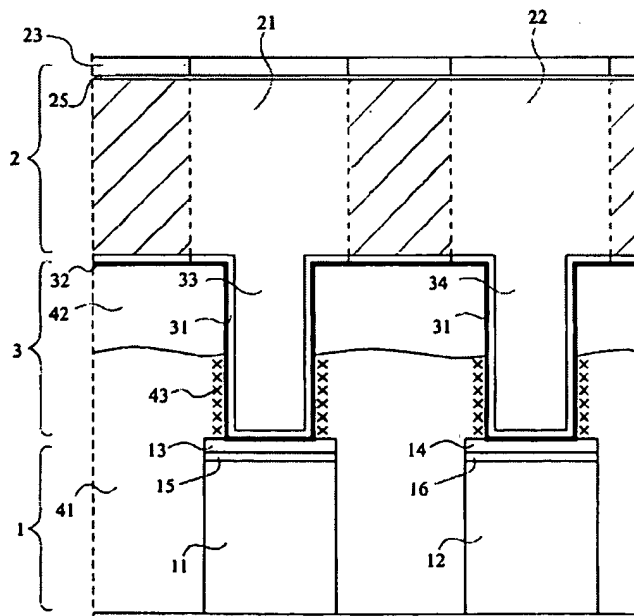
### Remarks

Claims 1, 2 and 4–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,180,520 ("Marty"). Claims 1–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,877,080 ("Aoi"). Claims 8–10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Marty in view of U.S. Patent 5,869,379 ("Gardener") or Aoi in view of Gardener.

#### **Claim Rejections Under § 102(e) based on Marty.**

Claims 1, 2 and 4–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,180,520 ("Marty"). Claims 1 and 5 are independent; Claims 2 and 4 depend from Claim 1, and Claims 6 and 7 depend from Claim 5.

Marty discloses an interconnect structure having a first metallization level 1 and a second metallization level 2, with vias 33, 34 connecting the two metallization levels. The first metallization level 1 includes two horizontally adjacent metallization "regions" or "portions" 11 and 12. Two distinct insulating layers 41 and 42 are disposed between the metallization levels. Specifically, a first insulating layer 41 having a relatively low dielectric constant contacts the first metallization level 1, while a second insulating layer 42 having a relatively high dielectric constant contacts the second metallization level 2. This structure is illustrated in Figure 1 of Marty, which is reproduced below.



In contrast to the structure disclosed in Marty, Applicant has amended Claim 1 to recite, among other limitations,

An interlevel dielectric directly contacting and formed between successive metallization levels in an integrated circuit, without other intervening materials between the successive metallization levels....

Marty does not teach this limitation. For example, in the Marty structure described and illustrated above, there is no interlevel dielectric that directly contacts, and that is formed between, the successive metallization levels. Specifically, in the structure disclosed in Marty, the first insulating layer 41 contacts only the first metallization level 1, and the second insulating layer 42 contacts only the second metallization level 2. There is no single interlevel dielectric that contacts both metallization levels. Applicant thus submits that Marty does not anticipate Claim 1, and therefore respectfully submits that Claim 1 is allowable over Marty. Furthermore, because Claims 2 and 4 depend from Claim 1, Applicant submits that Claims 2 and 4 are allowable over Marty for the same reasons that Claim 1 is allowable over Marty.

Likewise, Applicant has amended Claim 5 to recite, among other limitations,

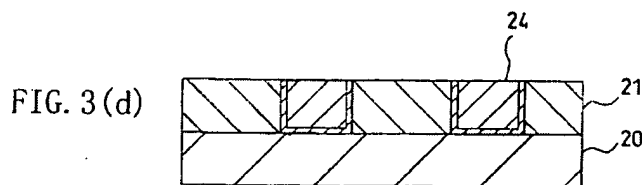
An integrated circuit having an electrical path, the integrated circuit comprising:  
a first, unitary metallization level providing a first portion of the electrical path;  
a second metallization level providing a second portion of the electrical path, the second metallization level separated from the first metallization level by a gap; and  
a single insulating layer directly contacting the first and second metallization levels and filling the gap between the first and second metallization levels....

Again, Marty does not teach this limitation. As described above, in the Marty structure there is no single insulating layer that directly contacts the first and second metallization levels. Rather, in the Marty structure, the first insulating layer 41 contacts only the first metallization level 1, and the second insulating layer 42 contacts only the second metallization level 2. Applicant thus submits that Marty does not anticipate Claim 5, and therefore respectfully submits that Claim 5 is allowable over Marty. Furthermore, because Claims 6 and 7 depend from Claim 5, Applicant submits that Claims 6 and 7 are allowable over Marty for the same reasons that Claim 5 is allowable over Marty.

**Claim Rejections Under § 102(e) based on Aoi.**

Claims 1–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,877,080 (“Aoi”). Claims 1 and 5 are independent; Claims 2–4 depend from Claim 1, and Claims 6 and 7 depend from Claim 5.

As characterized by the Examiner, Aoi discloses first and second conductive elements 24 separated from each other by a gap, with a single insulating layer 21 directly contacting the first and second conductive elements 24. This structure is illustrated in Figure 3(d) of Aoi, which is reproduced below.



In contrast to the structure disclosed in Aoi, Applicant has amended Claim 1 to recite, among other limitations,

An interlevel dielectric directly contacting and formed between successive metallization levels in an integrated circuit, without other intervening materials between the successive metallization levels....

Aoi does not teach this limitation. For example, in the Aoi structure described and illustrated above, there are intervening materials between the first and second conductive elements 24. Additionally, the Aoi structure's insulating layer 21 is not an interlevel dielectric, since the single insulating layer 21 does not contact successive metallization levels, but rather contacts conductors on the same level of the integrated circuit. Applicant thus submits that Aoi does not anticipate Claim 1, and therefore respectfully submits that Claim 1 is allowable over Aoi. Furthermore, because Claims 2–4 depend from Claim 1, Applicant submits that Claims 2–4 are allowable over Aoi for the same reasons that Claim 1 is allowable over Aoi.

Likewise, Applicant has amended Claim 5 to recite, among other limitations,

An integrated circuit having an electrical path, the integrated circuit comprising:  
a first, unitary metallization level providing a first portion of the electrical path;  
a second metallization level providing a second portion of the electrical path, the second metallization level separated from the first metallization level by a gap; and  
a single insulating layer directly contacting the first and second metallization levels and filling the gap between the first and second metallization levels....

Again, Aoi does not teach this limitation. As described above, the Aoi structure's insulating layer 21 is not an interlevel dielectric, since the single insulating layer 21 does not contact successive metallization levels, but rather contacts conductors on the same level of the integrated circuit. Applicant thus submits that Aoi does not anticipate Claim 5, and therefore respectfully submits that Claim 5 is in condition for allowance. Furthermore, because Claims 6 and 7 depend from Claim 5, Applicant submits that Claims 6 and 7 are allowable over Aoi for the same reasons that Claim 5 is allowable over Aoi.

**Claim Rejections Under § 103(a).**

Claims 8–10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Marty in view of U.S. Patent 5,869,379 ("Gardener") or Aoi in view of Gardener. Claims 8–10 depend from Claim 5.

Gardner does not teach the deficiencies of Marty and Aoi. Moreover, the horizontally separated elements disclosed in Gardner are not analogous to the vertically separated elements disclosed by Applicant. Specifically, Applicant has disclosed structures having a reduced dielectric constant without a cap layer, which relates only to vertically separated elements ("levels"), and is irrelevant to the horizontally separated elements taught by Gardner (and Aoi). See, for example, paragraphs [0057], [0058] and [0077] of the specification.

Because Claims 8–10 depend from Claim 5, Applicant respectfully submits that Claims 8–10 are allowable for the same reasons explained above with respect to Claim 5.

**Conclusion.**

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance, and respectfully requests the same. If, however, some issue remains that the Examiner feels can be addressed by an Examiner's Amendment, the Examiner is cordially invited to call Applicant's representative, Adeel S. Akhtar at (415) 954-4114 for authorization.

Respectfully submitted,

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Dated: 7-15-2003

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